Dimensional scaling of high-speed printed organic transistors enabling high-frequency operation

Gerd Grau[1] and Vivek Subramanian[2,3]

[1] Department of Electrical Engineering and Computer Science, York University, Toronto, Canada
[2] Institute of Microengineering, École polytechnique fédérale de Lausanne, Lausanne, Switzerland
[3] Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, USA

E-mail: grau@eecs.yorku.ca

Abstract

Printed electronics has promised to deliver low-cost, large-area and flexible electronics for mass-market applications for some time; however, so far one limiting factor has been device performance. Over the last decade, great progress has been made in terms of materials, processing and printing resolution for printed transistors. In this article, we review dimensional scaling of printed organic thin-film transistors (OTFTs), which has enabled high-frequency operation. We review different device architectures that require different dimensions to be scaled with accompanying tradeoffs in performance and complexity. Various printing methods have been used to print scaled transistors. Inkjet and gravure printing have seen the greatest improvements. We will focus on gravure printing here as it not only enables high-resolution features but also high-speed printing for low-cost manufacturing. Operating voltage has been scaled down less aggressively due to difficulties with scaling down the thickness of printed gate dielectrics. The performance of organic semiconductor materials has also improved substantially. When processing the semiconductor, the scaling of other device dimensions needs to be considered to optimize performance. Based on these advances, transistor switching frequency has increased dramatically over the last decade with several reports of high-speed printed inverters operating

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at high kHz to low MHz frequencies, which are promising results for emerging applications of printed electronics.

Keywords: Printed electronics, organic thin-film transistor (OTFT), dimensional scaling, high frequency, gravure printing, inkjet printing

1. Introduction

Printed electronics is a promising paradigm for microfabrication offering advantages over traditional silicon CMOS fabrication such as large-area compatibility, low cost and compatibility with flexible substrates including plastic and paper [1–4]. Many different applications have been suggested for printed electronics such as flexible displays [5], low-cost sensor networks [6] and item-level RFID tags [7]. At the heart of many of these applications are electronic circuits that contain transistors to perform tasks including switching in an active matrix, amplification of analogue signals and digital computation. Transistors have been printed from various materials including organic materials, inorganic metal oxides and carbon nanomaterials [8]. Whilst organic materials do not offer the highest performance, they are the most extensively studied class of materials in printed electronics due to the ease of processing them. Organic thin-film transistors (OTFT) typically contain organic materials (polymers and small molecules) for the semiconductor and gate dielectric layers and metal nanoparticles for the gate and source/drain electrodes. These materials can be dissolved in a multitude of organic solvents to formulate printing inks whose properties can be modified. Annealing temperatures are sufficiently low (on the order of 100°C) for fabrication on low-cost and flexible plastic substrates. In recent years, the challenge has been to improve the performance of OTFTs whilst simultaneously creating fully printed process flows that are

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compatible with low-cost manufacturing. In this article we will review our progress towards this goal over the last decade.

High-performance can be defined in different ways depending on transistor application. Assuming printed transistors will be used for switching applications at AC frequencies, the transition frequency (f_T) is a common metric to evaluate transistors' switching behavior. The transition frequency is defined as the frequency at which the current gain of the transistor driving a resistive load becomes unity. This frequency is relevant for both digital and analogue circuits as an upper bound on the frequency at which the circuit can be operated. It can be shown using a small-signal model that transition frequency is given by the following equation:

$$f_T = \frac{\mu(V_{GS}-V_{th})}{2\pi L\left(\frac{2}{3}L+2L_{overlap}\right)} \quad (1)$$

Transition frequency depends on semiconductor mobility (μ), gate-source voltage (V_{GS}), threshold voltage (V_{th}), channel length (L) and overlap length ($L_{overlap}$) between gate and source/drain. These factors can be sub-divided into material-dependent and dimensional factors. Mobility is the main material-dependent factor. Increasing mobility of printable organic semiconductors (OSC) has been a major area of research with a number of comprehensive review articles published [9–12]. Here, we will focus on dimensional factors. Transition frequency depends inversely on channel length and electrode overlap length. Therefore, scaling of the lateral dimensions will result in faster transistor operation. Another very important performance metric is power consumption. Printed transistors are most promising for mobile low-cost applications, which have very limited power sources. It is therefore very important to reduce the operating voltage of printed OTFTs, which has traditionally been very high. Important transistor characteristics that determine operating voltage are subthreshold swing (SS) and threshold voltage (V_{th}) i.e. characteristics that describe how much voltage is needed to turn on the transistor. Again, SS and V_{th} can be improved by materials innovation, such as high-k dielectrics or materials and interfaces with low trap densities, as well as dimensional scaling. In this case, the most

important scaling dimension is dielectric layer thickness. Scaling this dimension increases electric fields transverse to the channel, which means a smaller operating voltage can be used. It is therefore imperative to scale both lateral and thickness dimensions to achieve both high-performance and low-voltage operation. Dimensional scaling has been a major driver of the continued success of the silicon industry and has been formalized through the International Technology Roadmap for Semiconductors (ITRS) and the International Roadmap for Devices and Systems (IRDS). In printed transistors, scaling efforts have not been coordinated to nearly the same extent. Here, we review recent progress in dimensional scaling of OTFTs, which can guide future efforts.

Transistors have been printed using a multitude of different printing methods. Generally, there exists a trade-off between manufacturing throughput and resolution (see Figure 1). Here, we focus on high-throughput techniques that will enable low-cost manufacturing of large-area electronics and applications with large manufacturing volume. Manufacturing throughput (in m^2/s) is the product of printing speed and web width. Printing methods can be broadly classified as roll-based contact-printing and nozzle-based non-contact printing. Roll-based methods such as gravure, offset, flexography and screen printing generally offer high manufacturing throughput because they can operate at high print speed of several meters per second and can print on large webs that are several meters wide. Nozzle-based techniques such as inkjet printing require a large number of nozzles to cover a wide web. This increases the likelihood of nozzle clogging, which needs to be controlled carefully. An advantage of nozzle-based methods is that they are digital and designs can be changed on the fly for prototyping or low-volume manufacturing. There has been considerable effort to improve the resolution of these different techniques without compromising manufacturing throughput and achieve dimensional scaling of lateral transistor dimensions. Gravure printing in particular has achieved printed 2μm features at a print speed of 1m/s. The detailed printing physics to achieve this resolution has been reviewed elsewhere [13]. In order to fully consider manufacturing throughput, one needs to consider all processing steps, not just the

printing. Printed processes typically involve a substrate preparation step before printing as well as an annealing step after printing. Substrate preparation often involves plasma or UV ozone (UVO) treatment to increase substrate wettability. Annealing usually involves heating to dry off the ink solvent and induce processes such as crystallization or nanoparticle sintering. It is expected that printed electronics manufacturing will utilize scalable processes for these tasks such as atmospheric plasma treatment [14] or intense pulsed light (IPL) sintering [15]. Most research articles on highly-scaled printed OTFTs do not focus on manufacturing throughput in every step of the process and utilize methods that are difficult to scale such as vacuum-based plasma or hotplate annealing. Here, we will focus on fully-printed OTFT devices with highly-scaled electrodes that have been printed with high-speed printing methods. These reports demonstrate the potential for high-throughput manufacturing, although full high-throughput process flows will typically require further work. Reports will be classified by printing technology as a general representation of manufacturability but throughput won't be quantified further as it is not reported in most research articles.

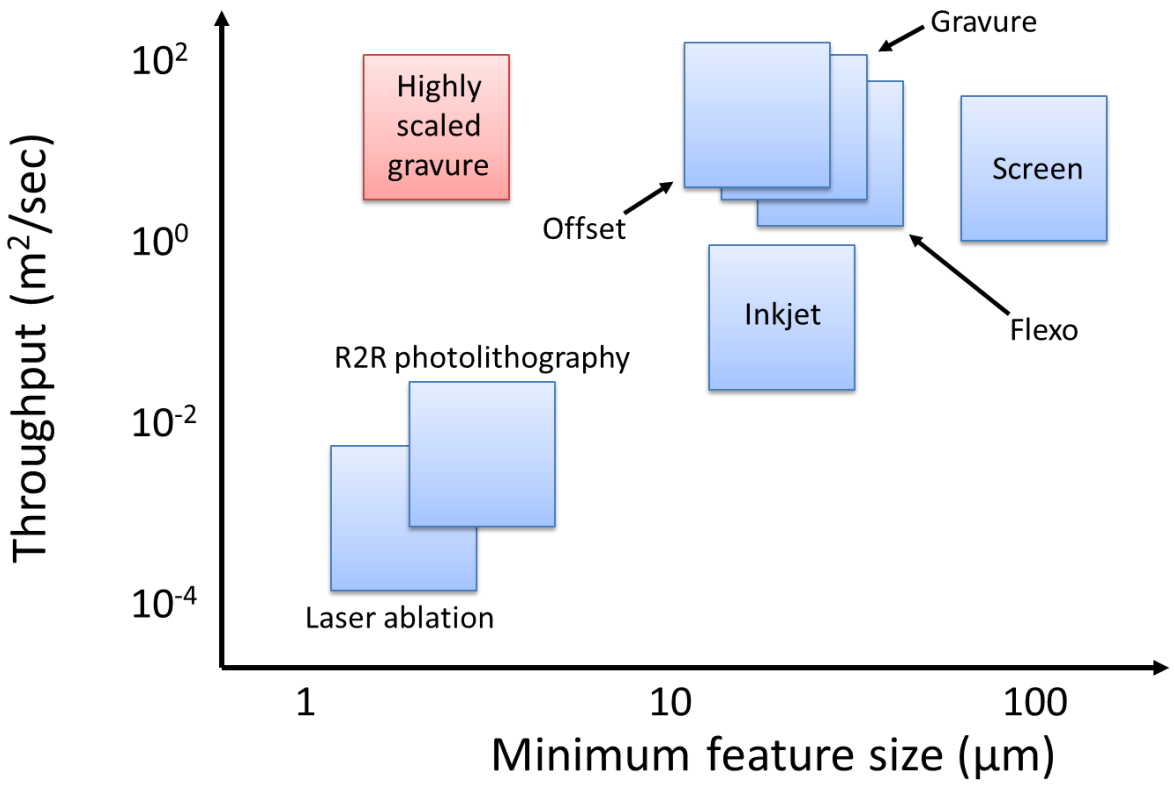


Figure 1. Overview of printing methods for printed electronics. Traditionally, there exists a trade-off between manufacturing throughput and resolution, which has been overcome by recent work in printed electronics. © IOP Publishing. Reproduced with permission from [13]. All rights reserved.

2. Electrode scaling and device architecture

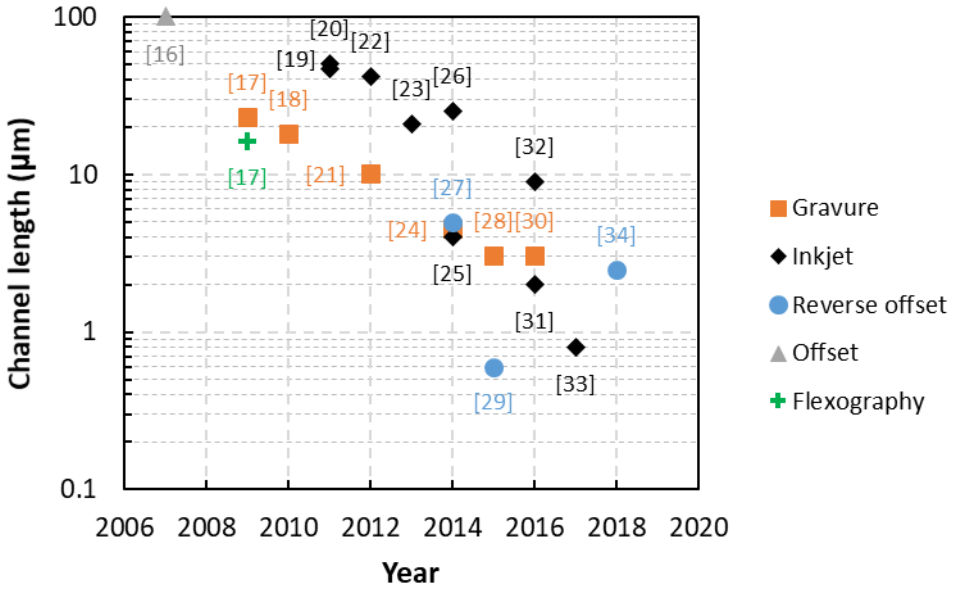
Figure 2 shows the electrode scaling trend in printed OTFTs over the last decade (for details see Table 1). For each printing method, the leading device at the time is plotted; leading in either channel length, overlap length or the geometrical factor that determines f_T:

Geometrical f_T factor $L_{fT} = L\left(\frac{2}{3}L + 2L_{overlap}\right)$ (2)

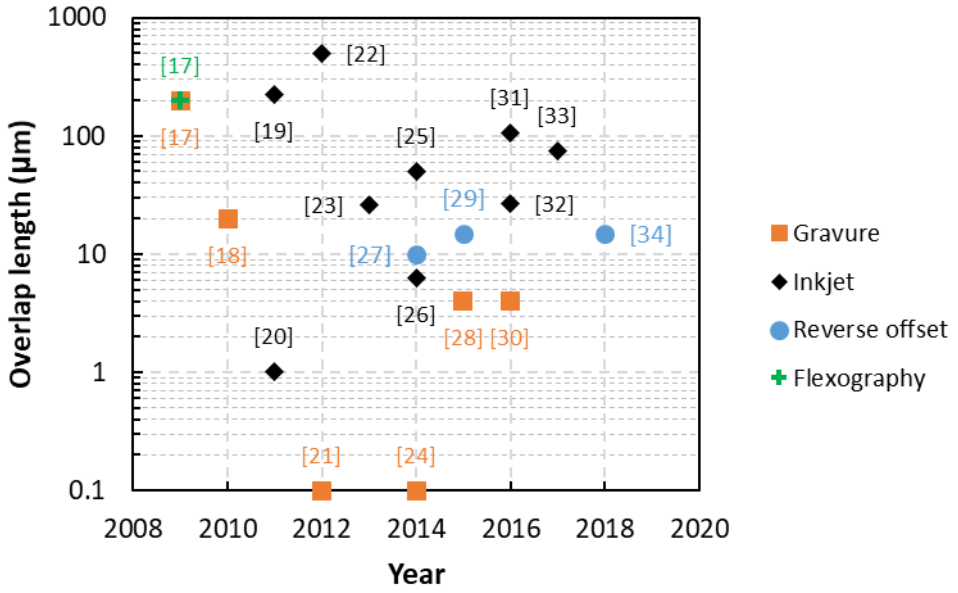
All devices shown are solution-processed and have printed electrodes. In cases where a combination of different printing methods was used (e.g. gravure for the gate and inkjet for source and drain), the device was classified by the printing method that was used for the critical dimension making it the leading device at the time. One can clearly observe an exponential trend. The two techniques that have

been developed most successfully are inkjet and gravure printing with inkjet lagging gravure printing. Recently, reverse offset printing has emerged as another promising method to print highly scaled OTFTs. It remains to be seen if reverse offset will undergo further downscaling. In the next section, we will describe some of the developments that have made this scaling possible and the trends that can be observed in more detail.

(a)



(b)



(c)

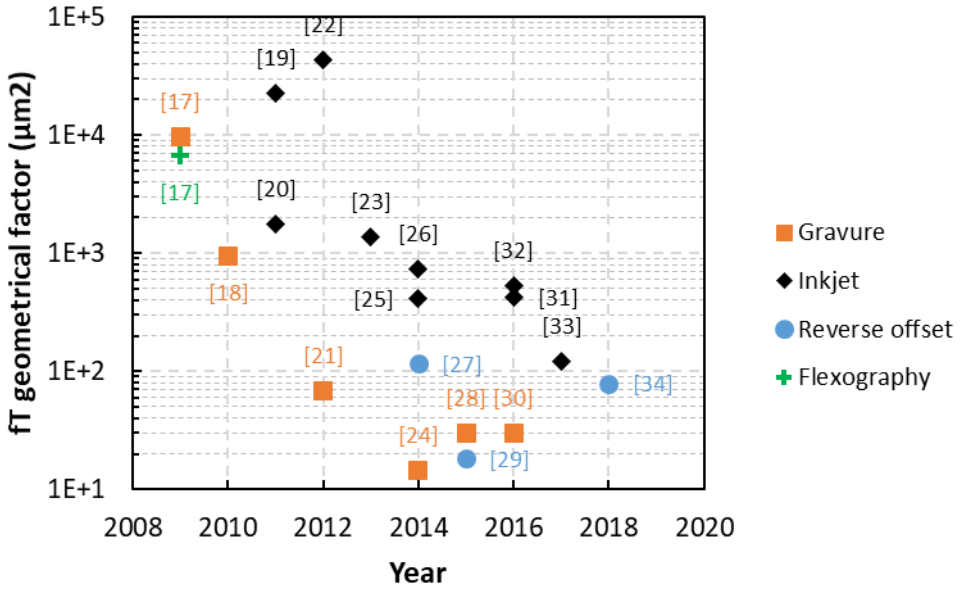


Figure 2. Historical development of printed OTFT scaling. An exponential trend can be observed for different printing methods and scaling metrics: (a) Printed channel length, (b) Printed overlap length between gate and source/drain, (c) Geometrical factor in f_T calculation combining the effects of channel length and overlap length.

Year	Reference	$L_{Channel}$ (µm)	$L_{Overlap}$ (µm)	L_{fT} (µm^2)	Printing method: S/D	Printing method: Gate	Printing method: Dielectric	Printing method: OSC	S/D to Gate Alignment	Structure	V_{Supply} (V)	f_T (Hz)	$f_{Inverter}$ (Hz)	OSC material	Mobility (cm^2/Vs)	Dielectric material	$t_{dielectric}$ (nm)
2007	[16]	100			Off	FG	GV	GV	FO	TG	60		27.8	F8T2	1.3* 10^{-3}	$BaTiO_3$	
2009	[17]	23.1	200	9.6* 10^3	GV	GV	SC	IJ	FO	BG	20			TIPS-Pentacene	8* 10^{-2}	PVP	400
2009	[17]	16.3	200	6.7* 10^3	FG	FG	SC	IJ	FO	BG	20			TIPS-Pentacene	8* 10^{-2}	PVP	400
2010	[18]	18	20	9.4* 10^2	IJ	GV	GV	GV	Al	BG	60	1.8* 10^4		pBTTT	6* 10^{-2}	PVP	
2011	[19]	47	225	2.3* 10^4	IJ	IJ	IJ	IJ	Al	BG	60			TIPS-Pentacene	2* 10^{-2}	PVP	900
2011	[20]	50	1	1.8* 10^3	IJ	IJ	IJ	IJ	Al	BG	40		10^2	TIPS-Pentacene	10^{-2}	PVP	110
2012	[21]	10	0.1	68.7	IJ	GV	GV	SC	Al	BG	25	3.1* 10^5		pBTTT	10^{-1}	PVP	160
2012	[22]	42	500	4.3* 10^4	IJ	SC	SC	DC	FO	BG	80			pBTTT	4* 10^{-2}	Teflon	260
2013	[23]	21	26	1.4* 10^3	IJ	IJ	SC	DC	Al	BG	20		40	pBTTT	3* 10^{-2}	PVP	490
2014	[24]	4.5	0.1	14.4	IJ	GV	GV	SC	Al	BG	5	3.5* 10^5	2* 10^5	lisicon® S1200	6* 10^{-2}	lisicon® D207	296
2014	[25]	4	50	4.1* 10^2	IJ	Ev	SC	DP	FO	BG	20		1.6* 10^4	lisicon® S1200	1.2	PVP	440
2014	[26]	25	6.25	7.3* 10^2	IJ	IJ	GV	SC	Al	BG	100			pBTTT	8.6* 10^{-2}	PVP	200
2014	[27]	5	10	1.2* 10^2	RO	RO	SC	RO	FO	BG	40			P3HT	10^{-2}	PVP	1000
2015	[28]	3	4	30	GV	IJ	GV	GV	FO	TG	20	1.9* 10^6		lisicon® S1200	8* 10^{-1}	lisicon® D139	200
2015	[29]	0.6	15	18.2	RO	IJ	CVD	IJ	FO	TG	20			diF-TES-ADT/PS	10^{-1}	Parylene	1000
2016	[30]	3	4	30	GV	GV	GV	GV	FO	TG	4	9.6* 10^4		lisicon® SP400	2* 10^{-1}	lisicon® D320	120
2016	[31]	2	106	4.3* 10^2	IJ	IJ	SC	SC	FO	TG	30			PDQT	6* 10^{-4}	PMMA	500
2016	[32]	9	26.8	5.4* 10^2	IJ	IJ	IJ	IJ	FO	TG	60		10^3	TIPS-Pentacene	6.5* 10^{-2}	PVP	1000
2017	[33]	0.8	75	1.2* 10^2	IJ	IJ	IJ	IJ	Al	TG	12			DPP-TT	2.7* 10^{-1}	PVP	350
2018	[34]	2.5	15	79.2	RO	RO	CVD	DP	FO	BG	2.5			diF-TES-ADT/PS	10^{-1}	Parylene	290

Table 1. Details of references in Figure 2. Abbreviations used: Geometrical f_T factor: L_{fT} (see equation (2)). Source and drain: S/D. Organic semiconductor: OSC. Offset: Off. Reverse Offset: RO. Gravure: GV. Inkjet: IJ. Flexography: FG. Spin coating: SC. Dispenser printing: DP. Drop casting: DC. Evaporation: Ev. Chemical vapor deposition: CVD. Fully overlapped structure: FO. Structure with gate aligned to source/drain: Al. Top-gate structure: TG. Bottom-gate structure: BG. Poly(9,9-dioctyl-fluorene-co-bithiophene): F8T2. 6,13-Bis(triisopropylsilylethynyl)pentacene: TIPS-Pentacene. Poly[2,5-

bis(3-dodecylthiophen-2-yl)thieno[3,2-b]thiophene]: pBTTT. Poly(3-hexylthiophene): P3HT. 2,8-Difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene blended with polystyrene: diF-TES-ADT/PS. Poly [3,6-bis(40-dodecyl[2,20]bithiophenyl-5-yl)-2,5-bis(2-hexyldecyl)-2,5-dihydropyrrolo[3,4-c]pyrrole-1,4-dione]: PDQT. N-alkyl diketopyrrolo-pyrrole dithienylthieno[3,2-b] thiophene: DPP-TT. Poly(4-vinylphenol): PVP. Poly(methyl methacrylate): PMMA. Product numbers of organic materials produced by EMD Performance Materials Corp.: lisicon® S1200, lisicon® SP400, lisicon® D207, lisicon® D139, lisicon® D320.

Thin-film transistors can be printed in a bottom-gate or top-gate configuration (see Figure 3). There are a number of considerations that determine the choice between these architectures. For example, some semiconductor materials show higher performance in one of the two configurations [35]. The choice of architecture fundamentally affects how scaled transistors are fabricated. In terms of scaling, typically, the most critical dimension is printed as the bottom layer. The bottom layer is printed directly onto the substrate, which can be cleaned and modified relatively freely using methods such as plasma treatment or a smoothing layer to improve wetting and surface roughness [26,36]. This is much more difficult for subsequent layers that need to be printed onto lower transistor layers. Higher layers in the transistor stack also need to be designed carefully to not damage underlying layers due to solvent interactions or thermal damage during annealing. Therefore, in bottom-gate transistors, the gate is typically the most highly scaled electrode. Conversely, in top-gate transistors, the source and drain electrodes are typically the most highly scaled electrodes. Similar considerations apply to the choice of whether to place source-drain electrodes underneath (bottom-contact) or on top of (top-contact) the semiconductor. Due to the difficulty of printing fine features onto the semiconductor without damaging it, bottom-contact architectures are much more common in fully printed transistors. All the highly scaled transistors in Figure 2 are bottom-contact.

There are two configurations in which the gate and the source-drain electrodes can be arranged laterally relative to each other: aligned and fully overlapped. In the aligned architecture, gate and source/drain electrodes are printed with minimal overlap (see Figure 3 (a) and (c)). In this case, channel length is defined by the width of the gate line. In principle, overlap length can be minimized close to

zero to maximize f_T. However, in practice, achieving good alignment has proven challenging especially for high-speed printing. This is partially due to the challenge of designing and manufacturing a printer that can repeatedly print with sub-micron alignment accuracy at printing speeds on the order of 1m/s. Additionally, flexible and low-cost substrates pose the fundamental challenge of potentially deforming during thermal treatments or due to web tension in a roll-to-roll process. Scaled and aligned transistors have therefore only been demonstrated using lower print speed methods. For example, source-drain electrodes have been inkjet-printed at low print speeds to align with a highly-scaled gravure printed gate [18,21,24]. This method has led to the smallest overlap capacitance to date for gravure printed OTFTs (see Figure 2 (b) in 2012 and 2014). However, it is challenging to achieve such alignment reliably. Devices or parts of devices can have a gap between the gate and the source or drain i.e. they exhibit underlap instead of overlap, which can be observed in Figure 4 (a). This adds series resistance to the device and limits on-current.

In order to achieve better alignment than possible by mechanical alignment of the printer, self-alignment has been investigated. Several studies have shown self-alignment within a layer to create a small gap between the source and drain electrodes i.e. a short channel [37–40]. Typically, the source electrode is printed first and its surface is subsequently rendered hydrophobic by applying a self-assembled monolayer (SAM). The drain electrode is printed partially over the source and will dewet from it due to the wettability contrast between the source and the substrate leaving a small gap between the source and drain electrodes. Small source-drain gaps can also be achieved in a step-edge architecture [41,42]. In this hybrid process, the source and drain metallization is performed by angled evaporation. The topography of the underlying gate blocks evaporated metal from being deposited on one of its edges thus forming the channel. This method can achieve small source-drain gaps but only one of the electrodes has a small overlap capacitance with the gate and it involves complex vacuum processing. Entirely vertical OFETs (VOFET) can be fabricated using printing. In this architecture, the

semiconductor is sandwiched between the drain and a percolating source with the gate underneath. The channel length is defined by the thickness of the semiconductor and can be very small. A challenge of this architecture is to maintain good gate control over the channel and good off-state performance. This requires a thin, high-quality gate dielectric, which is difficult to achieve by printing and is therefore typically deposited by non-printed methods [43,44]. These methods can be used to fabricate short-channel OTFTs but they do not solve the problem of overlap capacitance due to misalignment between the gate and the source/ drain electrodes. One method to address this is a self-aligned hybrid process where a photoresist is patterned by exposing it to light from the backside of the sample. The first electrode layer acts as a photomask to achieve self-alignment. The first electrode layer can be fabricated by a range of methods including nanoimprint lithography [45–47], roll-to-roll photolithography [48] and self-aligned printing of source-drain electrodes [38]. This method can achieve very small overlap capacitance; however, requires additional processing steps such as photoresist development or lift-off after metal evaporation. A one-step printed method to achieve layer-to-layer self-alignment has been demonstrated exploiting differences in wettability [20]. The gate is printed first followed by the gate dielectric. The source and drain electrodes will wet the area around the gate but not directly over the gate leading to a minimal overlap area (see Figure 4 (b)). This method is the best to-date in terms of overlap for inkjet-printed OTFTs (see Figure 2 (b) in 2011). A related method uses embossing to pattern the source-drain electrodes on either side of a groove. Self-alignment is achieved by making the substrate outside of the groove hydrophobic and confining the gate ink to the groove [49]. However, it is challenging to achieve the required surface energy differences reliably and it has not been demonstrated for a high-speed printing technique such as gravure. One problem is that roll-based techniques tend to use higher-viscosity inks than inkjet, which inhibits any flow necessary for self-alignment. If the gate is inkjet-printed, the channel length is limited by the linewidth of the inkjet-printed gate line. In inkjet printing, linewidth is directly correlated with nozzle diameter, which is difficult to scale down. Smaller

nozzles are prone to clogging thereby reducing printing yield. This problem can be circumvented by careful control of the ink on the substrate. Recent work has reported 14μm inkjet-printed linewidth on a non-crosslinked SU-8 buffer layer [50]. The utility of these lines in printed transistors remains to be demonstrated. Because of these challenges, many recent reports have utilized a fully overlapped structure.

In the fully overlapped architecture, the gate electrode is significantly wider than the channel length (see Figure 3 (b) and (d)). In this case, channel length is defined by the separation between source and drain. Overlap length is defined by the width of the source and drain electrodes. The structure is misalignment tolerant as long as the gate is large enough to always overlap the channel fully. This simplifies fabrication as no strict alignment is necessary. There is also only one critical layer, source and drain, which needs to be optimized. This method has been applied for both gravure and reverse-offset printing, the two most highly scaled printed electronics methods. Gravure printing has undergone a transition from utilizing the aligned structure to the fully overlapped structure (see Figure 4 (c) for an example). This can be observed in Figure 2 (b) where the overlap length has increased recently as a result of this transition. However, the f_T geometrical factor did not increase as much due to continued scaling of the channel length and the use of scaled source and drain electrodes in the fully overlapped architecture. Scaled printing of narrow linewidth source and drain electrodes is crucial for this architecture. Every printing method has its own challenges and limitations as feature size is scaled down. Inkjet printing is limited by nozzle size and clogging as described above. In gravure printing, the pattern is defined by a series of recessed cells that are engraved into the surface of the master roll. A limiting factor is the volume of ink that is transferred from each cell. Fundamentally, cell volume is reduced as lateral cell area is scaled down because cell depth cannot be scaled up proportionally. This can lead to very thin and disconnected lines. To maximize the ink volume that is transferred to the substrate, there is a need to optimize every step in the gravure process. This begins, for example, with using silicon

microfabrication to create a roll with very precise features whose properties can be tuned [51]. A deep understanding of the fluid mechanics involved in printing is necessary to find the optimum printing conditions. In gravure printing, most phenomena can be understood by considering the non-dimensional capillary number that describes the balance between viscous and surface tension forces as a function of ink viscosity, print speed and ink surface tension [52,53]. Doctor blade wiping to remove excess ink from land areas between cells is a crucial process. If not optimized, it can create defect streaks that can destroy circuits. The doctor blade can also remove ink from cells and deposit it behind cells which can distort patterns and reduce ink volume in patterns. To solve these issues, the shape and surface properties of the doctor blade can be optimized in conjunction with optimizing printing parameters [54–57]. By understanding and optimizing these various aspects of the gravure process, we have achieved 2µm features by gravure printing that were employed in fully-printed OTFTs [28,30]. The details of the gravure process have been reviewed in greater detail elsewhere [13].

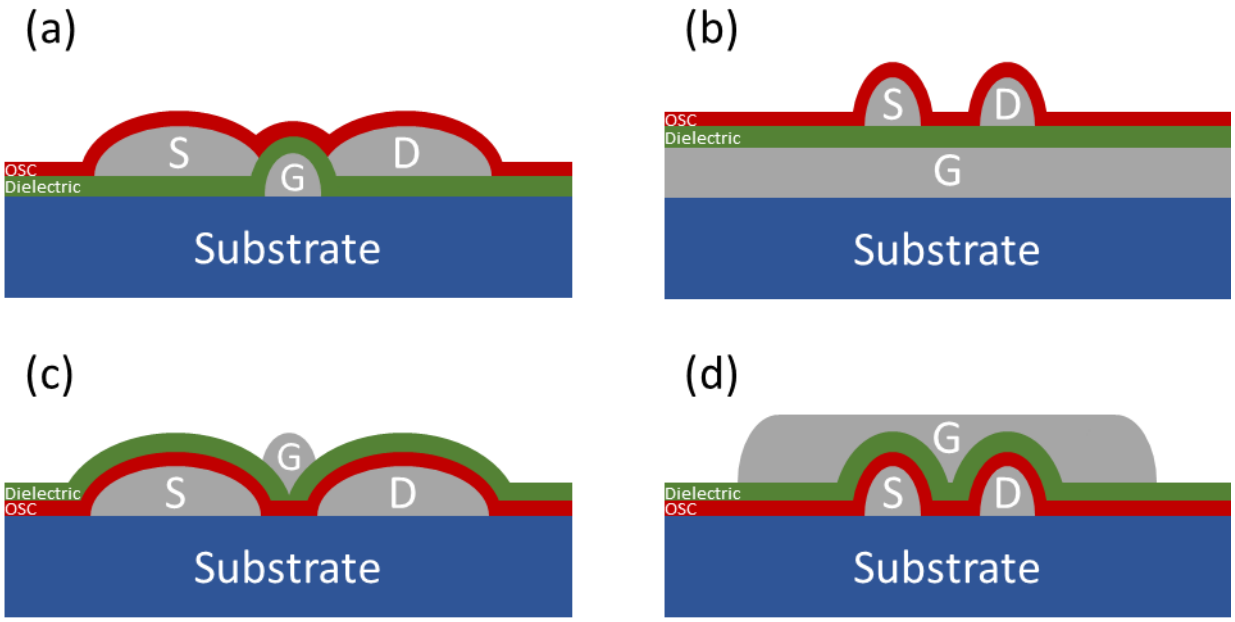
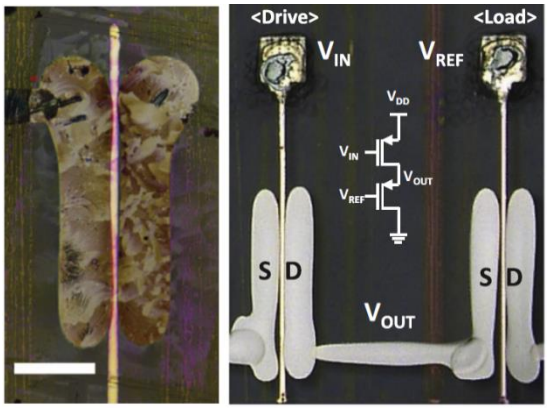
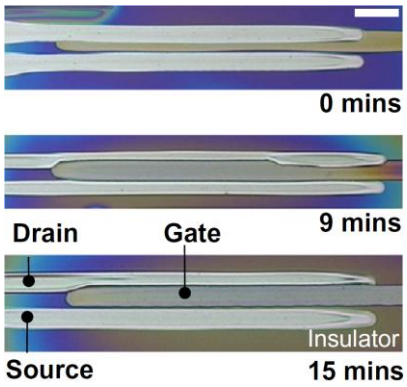


Figure 3. Cross-sections of most common printed OTFT device structures: (a) Bottom-gate aligned, (b) Bottom-gate fully overlapped, (c) Top-gate aligned, (d) Top-gate fully overlapped

(a)



(b)



(c)

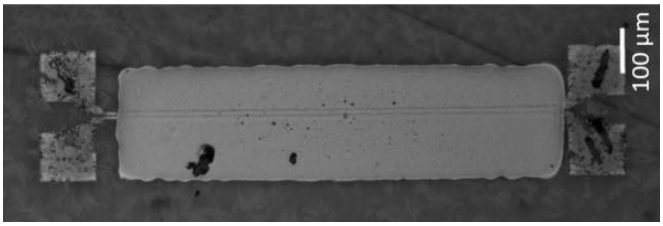


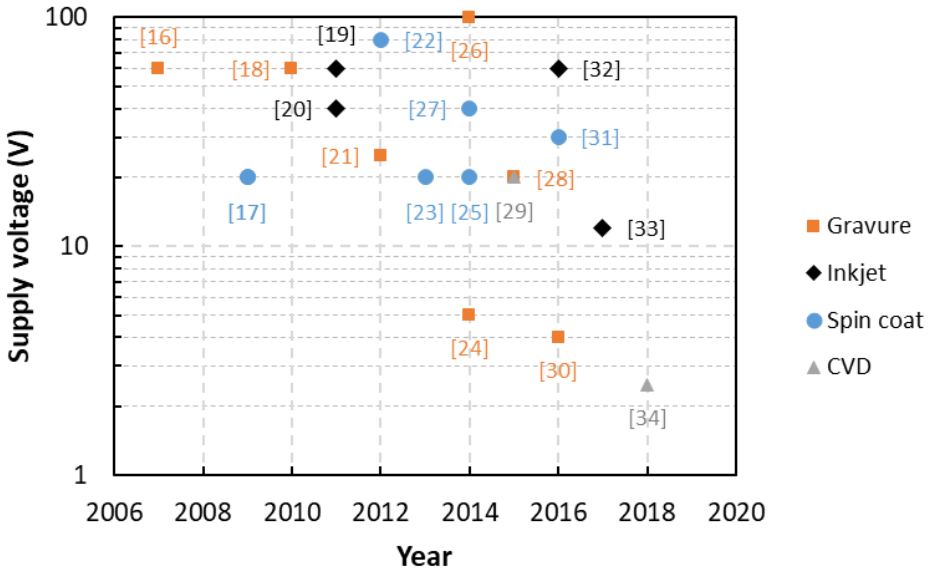
Figure 4. (a) Bottom-gate OTFT with highly scaled gravure-printed gate line and aligned inkjet-printed source and drain. Regions with good alignment and minimal overlap capacitance as well as regions with underlap can be observed. Reprinted from [24], with permission from Elsevier. (b) Self-alignment process. The inkjet-printed source and drain electrodes at first overlap with the gate. They gradually dewet due to differences in surface energy leading to minimal overlap capacitance. Reprinted from [20], with permission from Elsevier. (c) Fully overlapped top-gate OTFT with highly-scaled gravure-printed source and drain electrodes and inkjet-printed gate. Overlap capacitance is minimized by the narrow width of the source and drain lines. Reprinted with permission from [28] © 2015 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. All scale bars represent 100µm.

3. Gate dielectric and operating voltage scaling

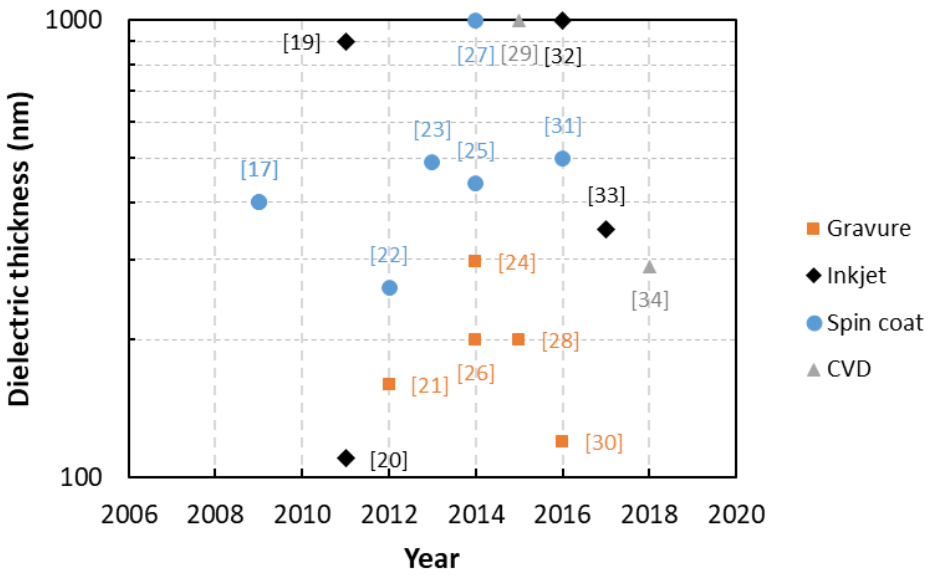
As channel length is scaled, the lateral electric field increases, which allows voltage to be scaled as well. This is very important in printed organic transistors whose operating voltage is traditionally very high on the order several tens of volts. This is especially detrimental in low-cost, mobile applications, which are expected to have very limited power sources. Figure 5 (a) shows that there is a trend towards lower supply voltage for scaled printed OTFTs but it is not as clear as for scaling of lateral feature size. Recently, there are some reports of relatively low-voltage transistors with sub-10V operation. However, there are still many reports of transistors operating at higher voltages. The reduction of operating voltage is mainly limited by the turn-on behavior of transistors, namely subthreshold swing and threshold voltage. It is not uncommon for OTFTs to exhibit a subthreshold swing of several volts per decade, which necessitates a large supply voltage to turn the transistor on. Subthreshold swing can be reduced by optimizing the semiconductor and the semiconductor-dielectric interface to reduce charge carrier trap density. A more direct way is to increase the gate dielectric capacitance, which can be achieved by downscaling the dielectric thickness or increasing the dielectric constant. High-k gate dielectrics have been employed in printed OTFTs [58]. However, the vast majority of scaled printed OTFTs employ low-k polymeric gate dielectrics. One reason is that the increased polarity of high-k dielectrics can adversely affect charge transport in the semiconductor thus leading to reduced mobility and on-state performance [59]. Figure 5 (b) shows the historical scaling trend of dielectric thickness and one can observe that there is no clear trend. Dielectric thickness tends to vary between 100nm and 1μm. There are very few reports that have scaled both lateral feature size and dielectric thickness. When considering different reports of scaled transistors, the correlation between dielectric thickness and operating voltage is not as strong as one would expect (see Figure 5 (c)). This is the case because the materials and processing conditions vary wildly between different reports and many did not optimize for low voltage. It is more instructive to consider the effect of dielectric scaling on subthreshold swing and threshold voltage for a single system

where all other parameters are held constant. In this case, the expected trend can be observed (see Figure 6). If the operating voltage is scaled proportionally with dielectric thickness (constant field scaling), the shapes of transistor transfer curves look very similar (see Figure 7). As operating voltage is scaled at the same rate as subthreshold swing and threshold voltage, the transistors turn on over the same fraction of the maximum V_{GS}. On-current is reduced in this scaling regime as expected assuming the OTFT follows MOSFET square law theory (or even more strongly, since disordered semiconductors often show an increase in mobility with carrier concentration due to trap filling). Current scales approximately quadratically with voltage but only linearly with inverse dielectric thickness and W/L is constant. This is beneficial as it reduces power consumption of circuits. One can observe a difference in gate leakage depending on dielectric thickness. Even though the electric field is constant, gate leakage increases with thinner dielectrics. This problem has limited dielectric scaling in printed OTFTs. There are several challenges that need to be overcome.

(a)


100
10
1
Supply voltage (V)
2006
2008
2010
2012
2014
2016
2018
2020
Year
[16]
[19]
[22]
[26]
[18]
[32]
[20]
[27]
[31]
[21]
[28]
[17]
[23]
[25]
[29]
[33]
[24]
[30]
[34]
Gravure
Inkjet
Spin coat
CVD

(b)


1000
100
Dielectric thickness (nm)
2006
2008
2010
2012
2014
2016
2018
2020
Year
[19]
[27]
[29]
[32]
[23]
[31]
[25]
[17]
[33]
[22]
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[30]
[20]
Gravure
Inkjet
Spin coat
CVD

(c)

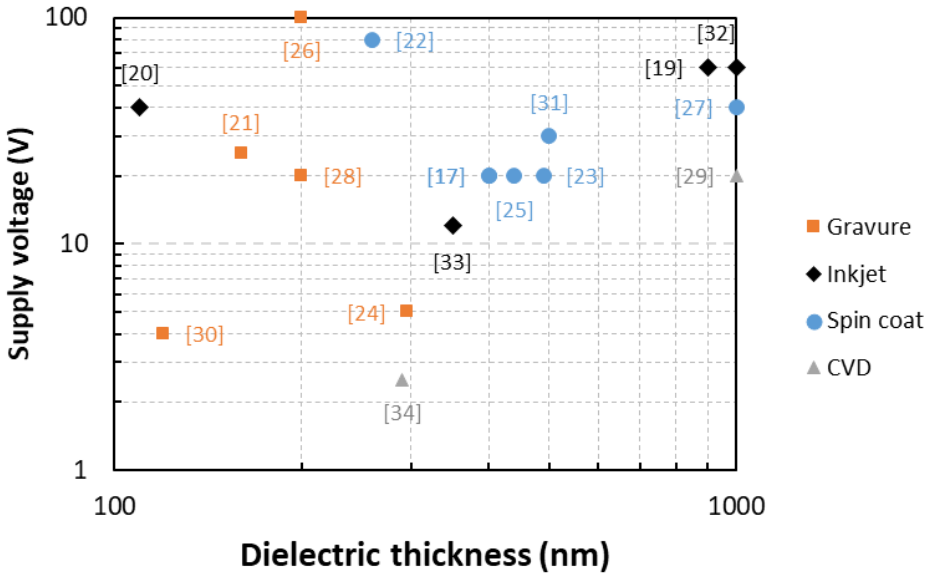


Figure 5. Dielectric scaling by dielectric printing method. (a) Downscaling trend of supply voltage is less clear than scaling trend of lateral dimensions. (b) This can be partially explained by the fact that gate dielectric thickness does not follow a clear scaling trend. (c) Correlation between supply voltage and dielectric thickness is weak due to other material-dependent factors that affect operating voltage.

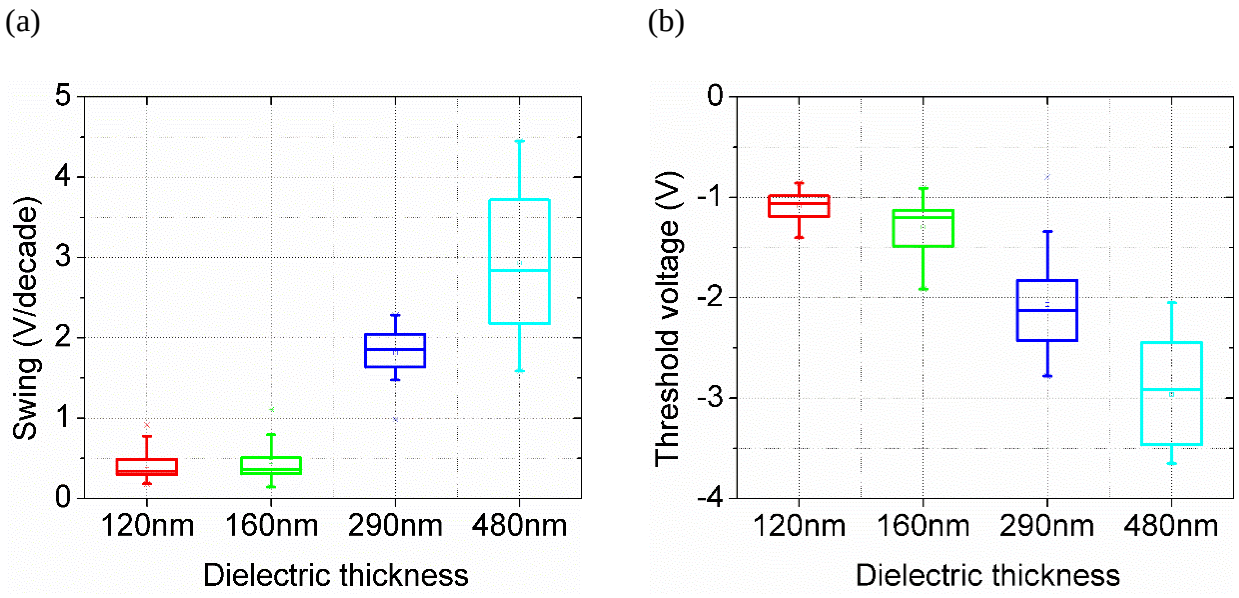


Figure 6. If all other device parameters are kept constant, (a) subthreshold swing and (b) threshold voltage follow the expected trends with downscaling of gate dielectric thickness. Reprinted with permission from [30] © 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

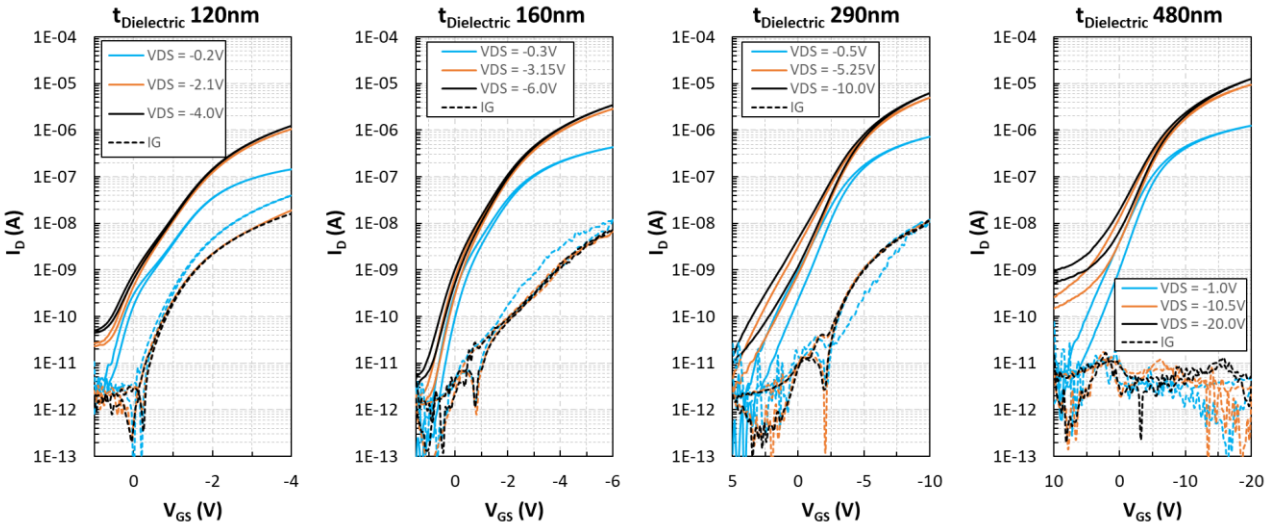


Figure 7. Transfer curves for transistors with different dielectric thickness that are otherwise identical. Operating voltage is scaled proportional to gate dielectric thickness. Curve shape stays constant except for reduced on-current with low supply voltage. Gate leakage increases for thinner dielectric. All layers were gravure printed. Dielectric: D320. Semiconductor: SP400. Channel length=5µm. Fully overlapped architecture.

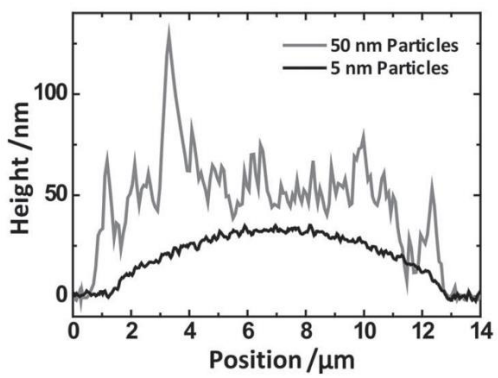
One challenge is the surface roughness of the layer underneath the gate dielectric. Electrodes in printed OTFTs are typically fabricated using metal nanoparticle inks as these deliver good printability and high conductivity at low processing temperatures [60–62]. Even after sintering, nanoparticle films retain significant surface roughness, which can be on the order of tens of nanometers. If a very thin dielectric is printed on top of such films, metal peaks will lower the effective dielectric thickness and increase electric field leading to increased gate leakage and breakdown. The magnitude of surface roughness is of the same order as the size of the metal nanoparticles and can therefore be reduced significantly by decreasing the size of the nanoparticles (see Figure 8 (a)) [21]. Roughness can also be minimized by optimizing sintering conditions. The coffee ring effect can also create unwanted surface topography [63], which could increase gate leakage. Nowadays, many commercial metal nanoparticle inks for inkjet printing have been formulated to suppress coffee ring. Gravure-printed electrodes normally don't face this problem because metal nanoparticle ink viscosity is an order of magnitude larger than in inkjet, which suppresses the flow that causes coffee ring. Bottom-gate TFTs are more affected by surface roughness because the gate dielectric is printed directly onto the gate electrode. In top-gate transistors, the gate dielectric is printed onto the organic semiconductor, which typically exhibits less surface roughness.

Another difficulty is the printing of the gate dielectric itself. One can note in Figure 5 that a significant number of articles reporting transistors with scaled printed electrodes use spin coating to deposit the gate dielectric and some use chemical vapor deposition (CVD) of parylene. These methods are not scalable for high-speed, low-cost manufacturing and films cannot easily be patterned; however, they are convenient for device level research and prototyping. It is more difficult to achieve a uniform thickness when printing a thin gate dielectric. Non-uniformities can increase gate leakage and, in the worst case, pinholes can reduce yield. For example, in gravure printing, ink is transferred to the substrate as droplets from discrete cells with a finite gap in between. Ink needs to spread on the substrate to create a uniform

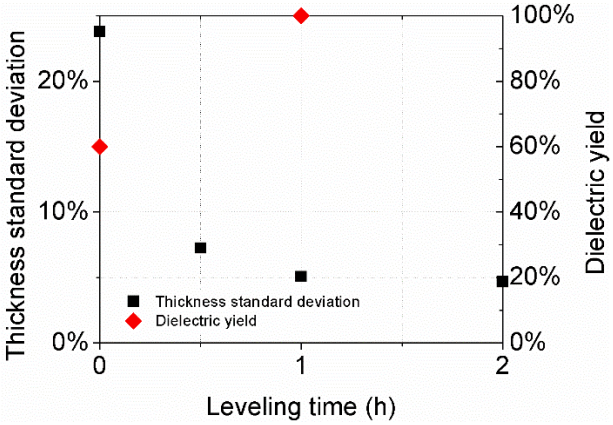
film. This can be aided by increasing the surface energy of the substrate. Thickness variations can also be induced by non-idealities in the gravure printing process such as ink squeezing between the roll and the substrate [64] or the Saffman-Taylor instability [65–67]. These undulations can be smoothed out by surface tension forces if there is enough time during the drying process before the ink becomes solid. The leveling process can be accelerated by a mixture of co-solvents that induces a surface tension gradient [28] or by decreasing ink viscosity [68], although lower viscosity can lead to thinner films and less well defined patterns. Alternatively, the drying process can be slowed by using a lower vapor pressure solvent or by allowing the film to level in a solvent atmosphere before drying (see Figure 8 (b)) [30].

Another challenge is the printing of the subsequent layer on top of the gate dielectric, for example the gate in the top-gate architecture. If all layers are solution-processed, one needs to ensure that all layers have orthogonal solvents. In particular, a thin dielectric layer can easily be penetrated by a subsequent conductive layer leading to short circuits and diminished yield. Therefore, the materials and solvents for the entire device stack need to be designed as a comprehensive system. Solvent selection can be aided by Hansen solubility parameters, which describe solubility in terms of three orthogonal energy components: dispersion (nonpolar forces), polarity (dipole forces) and hydrogen bonding [69]. However, it can be difficult to design such a comprehensive system given the other constraints on OTFT materials such as printability, patterning and electrical properties. Optimization of drying conditions can help to reduce the impact of incompatible solvents. If the gate solvent only moderately dissolves the underlying gate dielectric, a significant reduction in pinholes can be achieved by separating the gate drying and sintering steps using a two-step heat treatment. First, the solvent is dried off at a low temperature, which reduces the rate at which the gate solvent dissolves the dielectric. Drying can be accelerated by drying under vacuum. Second, the gate is sintered at a higher temperature to improve conductivity. Since the solvent has already evaporated, it cannot attack the dielectric anymore (see Figure 8 (c)) [70].

(a)



(b)



(c)

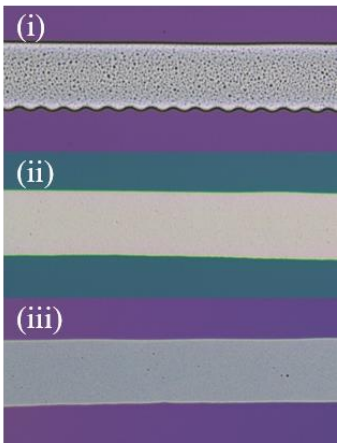


Figure 8. (a) Smaller nanoparticles greatly reduce surface roughness of metal electrodes, which prevents breakdown of the dielectric printed as the next layer. Reprinted with permission from [21] © 2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (b) Levelling the dielectric film in a solvent atmosphere after gravure printing before drying significantly reduces thickness non-uniformities and improves dielectric yield. Reprinted with permission from [30] © 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (c) (i) Solvent interaction between a printed silver gate and the underlying dielectric during gate sintering can lead to pinholes in the dielectric (black dots). (ii) Drying at 30°C in vacuum prevents pinholes from forming. (iii) Further high-temperature sintering to increase conductivity does not result in the creation of pinholes. Reprinted from [70].

4. Semiconductor scaling

The organic semiconductor (OSC) is the layer that is least well described in terms of dimensional scaling because its behavior depends very strongly on the material's chemical structure and processing conditions. A large number of organic semiconductors have been reported over recent years with increasingly high performance including a number of printable semiconductors. Reports of scaled transistors have utilized a smaller subset of these materials (see Figure 9). Mobility, which is the most important material property for high-frequency operation, has increased by several orders of magnitude over the last decade. Mobility is very strongly correlated with the OSC material. Nevertheless, mobility can vary by up to an order of magnitude between reports using the same OSC material. In order to achieve the full potential of a material, processing conditions and device design need to be optimized. Here, we will focus on challenges that arise as a consequence of dimensional scaling of the other OTFT layers. Depending on material, device scaling can either increase or decrease mobility.

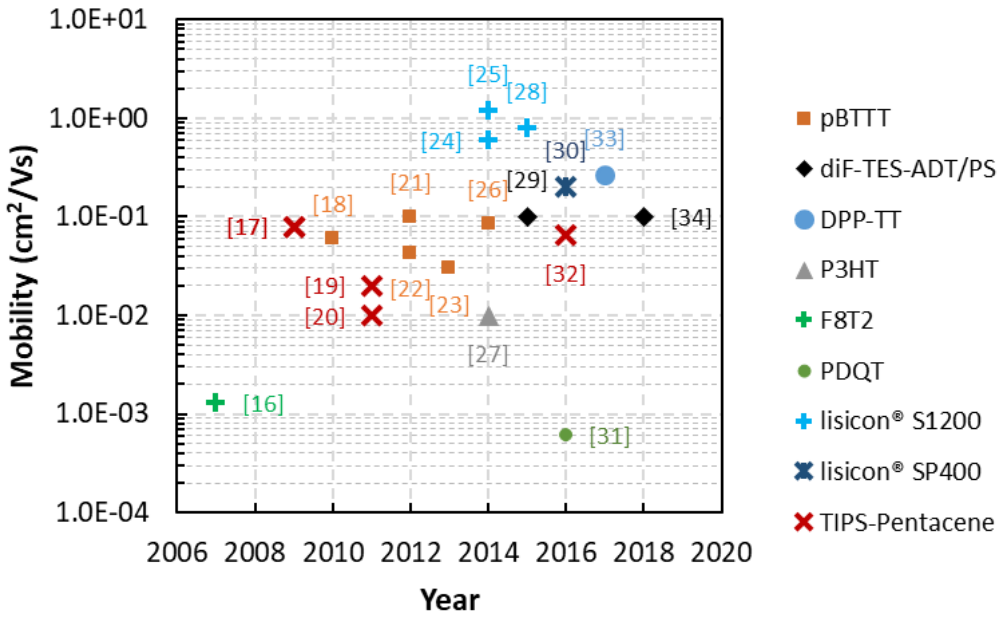
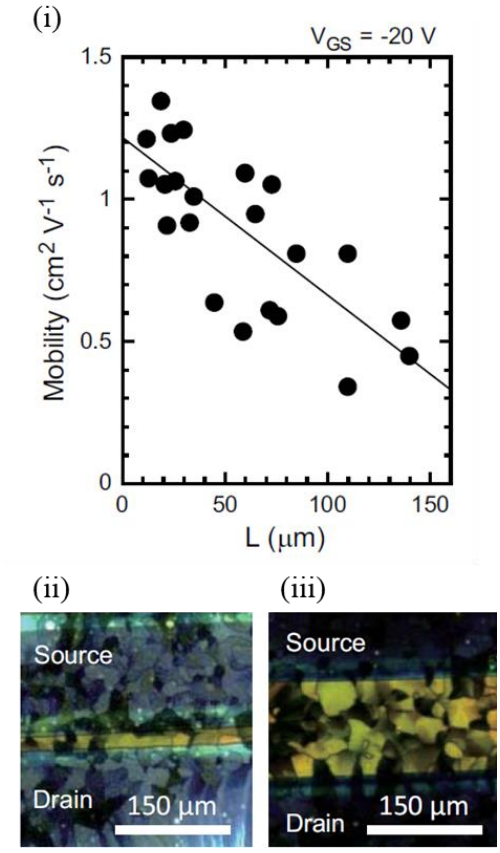


Figure 9. Organic semiconductor mobility in printed transistors has increased dramatically over the last decade. Mobility is very highly correlated with material but one can observe variations of up to one order of magnitude for the same material depending on processing conditions and device structure.

Many high-performance organic semiconductors are polycrystalline. Device performance depends strongly on crystallite size and quality. Charge transport is most efficient within grains. Conduction is typically limited by grain boundaries. If channel length is scaled down sufficiently to be of the same size as the OSC grains, transport can resemble transport through a single crystal. In this case, mobility is increased as channel length is scaled down (see Figure 10 (a)) [71], though this will likely be achieved at the expense of device-to-device uniformity. The opposite trend can be observed if the source and drain electrodes disturb crystallization. The source and drain electrodes are typically printed before the semiconductor (bottom-contact architecture). Due to the difference in surface energy and surface roughness between the metal nanoparticle electrodes and the surrounding area, the organic semiconductor can crystallize preferentially on the electrodes. This leads to small grains with large disorder on top of the electrodes with larger grains growing into the channel. Shorter channels are affected more by this disorder compared with longer channels that have large grains at the center of the channel (see Figure 10 (b)). In this case, mobility is larger for longer channels [72]. The dependence of crystallization and mobility on channel length can also increase variability if there is variability in printed channel length. It also needs to be considered when designing circuits consisting of devices with various channel lengths. This problem is not present for amorphous semiconductors. Traditionally, amorphous polymer semiconductors have lagged behind small-molecule polycrystalline semiconductors in terms of mobility; however, significant progress has been made making amorphous OSCs a viable alternative [30,73].

(a)



(b)

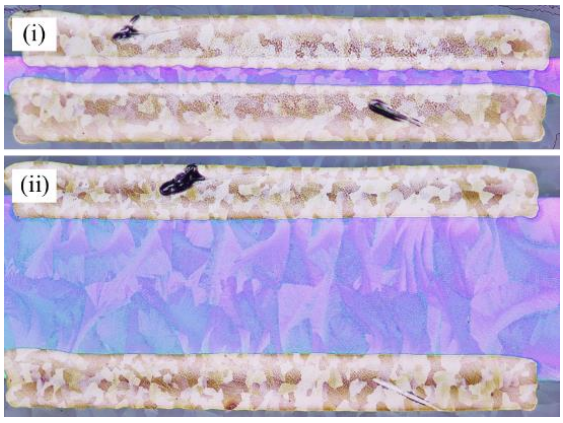
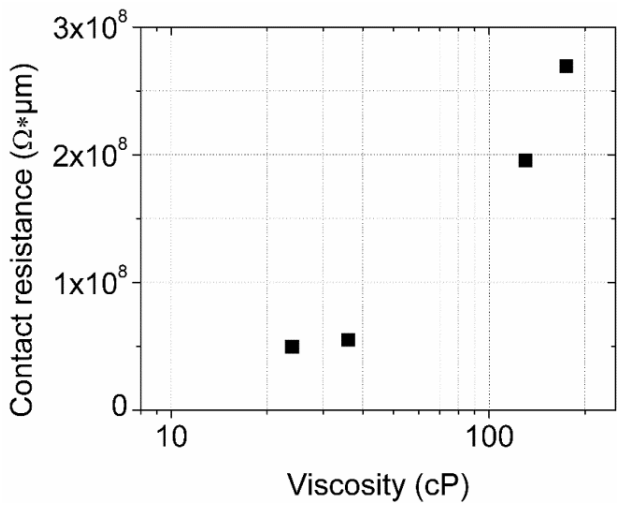


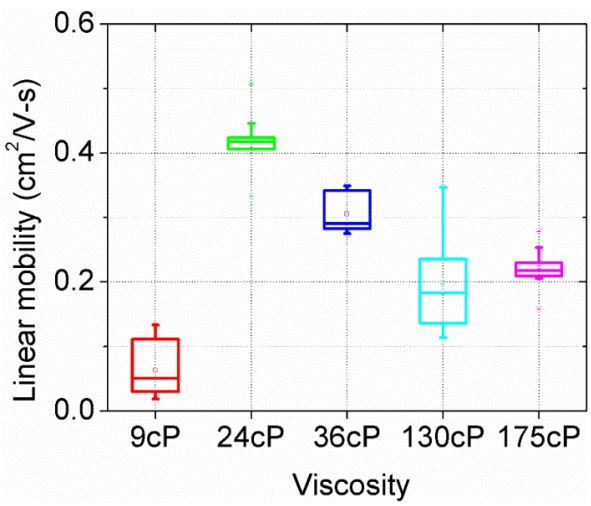
Figure 10. (a) (i) Mobility increases with decreasing channel length in polycrystalline semiconductors when grains can bridge (ii) short channels but not (iii) long channels. Reprinted from [71] under a Creative Commons Attribution 3.0 Unported License. (b) Conversely, grains can preferentially nucleate on the source and drain electrodes leading to small grains over the electrodes and larger grains at the centre of the channel. In this case, (i) short channel transistors have lower mobility ($0.086cm^2$/V-s) than (ii) long channel transistors ($0.26cm^2$/V-s). Reprinted from [72], with permission from Elsevier.

Irrespective of crystallization, shorter channel transistors are affected more severely by contact resistance. Due to a mismatch between the work function of the electrodes and the HOMO level of the p-type semiconductor, a contact barrier is often present in OTFTs. As transistors are scaled, channel resistance decreases but contact resistance is unchanged leading to decreased effective mobility. A contact barrier can also lead to an overestimation of mobility when not accounted for during mobility extraction [74]. A common strategy to solve this problem is to increase the work function of the electrodes by adding an interlayer such as a self-assembled monolayer (SAM) [75,76] or a thin metal oxide layer [77]. The work function of printed silver nanoparticle electrodes can also be increased by exposing them to a short plasma treatment, which can be combined with a SAM treatment [24]. In top-gate bottom-contact transistors another problem is that the source and drain electrodes are at the bottom of the semiconductor film, however, the channel is at the top of the film. This means that charge carriers need to be conducted through the thickness of the semiconductor film, which is not accumulated by the gate field and whose resistance is therefore high. The solution for this problem is to scale down the thickness of the semiconductor, which decreases contact resistance and increases effective mobility (see Figure 11 (a) and (b)) [30]. Thickness can be scaled down most easily by reducing the semiconductor concentration in the ink. This also reduces ink viscosity, which can detrimentally affect pattern fidelity (see Figure 11 (c)). Patterning of the semiconductor is important to remove leakage current paths and to print circuits with multiple isolated devices. It is therefore important to design the ink, printing parameters and device structure in conjunction. Similar considerations apply to the printing of the semiconductor as the gate dielectric, which both need to be printed as thin, defect-free films.

(a)

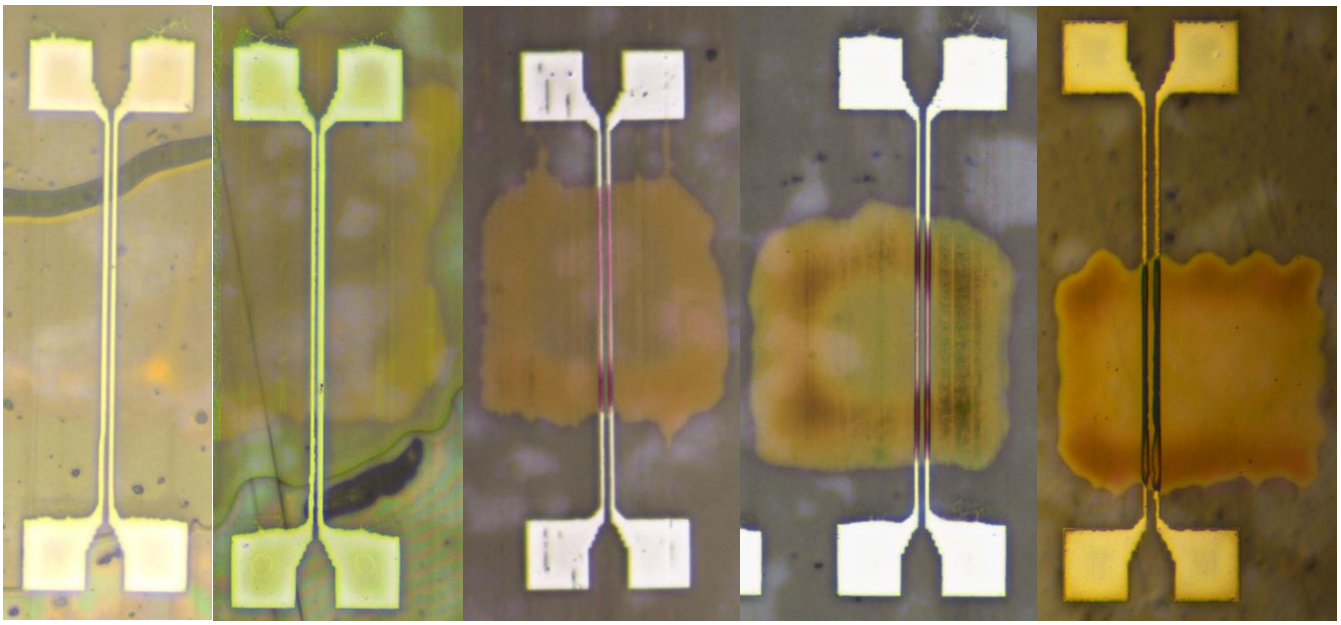


(b)



(c)

9cP 24cP 36cP 130cP 175cP



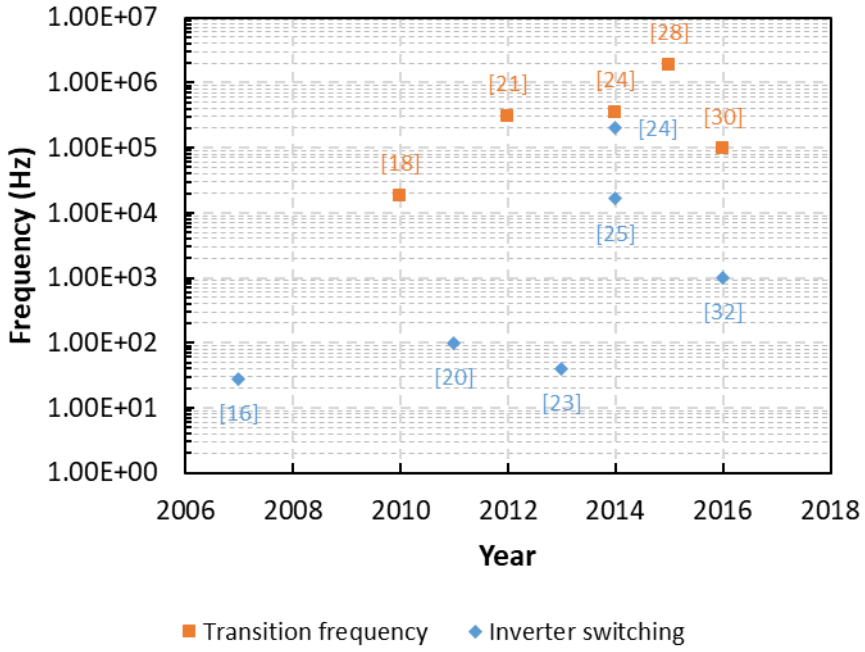
30µm

Figure 11. (a) In top-gate bottom-contact OTFTs, contact resistance decreases when the thickness of the semiconductor film is reduced by reducing the semiconductor concentration and viscosity of the ink. (b) Effective linear mobility increases as a result of the decreased contact resistance, except when the viscosity is too low and the film becomes too thin to sustain substantial current. (c) However, pattern fidelity decreases with decreasing viscosity of the semiconductor ink. Reprinted with permission from [30] © 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

5. High-frequency operation

All of the above considerations combined determine the switching speed of the final device. Figure 12 (a) shows the historical trend of switching speed in scaled printed OTFTs. One can observe an exponential trend with improvements over several orders of magnitude in recent years. Switching speed tends to be reported in two different ways in the literature. One method is transition frequency where the transistor drives a resistive load in an inverter configuration and f_T is the frequency at which current gain becomes unity. This is an analogue method with a sinusoidal input. Transition frequency signifies the upper frequency limit at which this transistor can operate. The other method uses a second printed transistor as the load in an inverter configuration. A digital signal (square wave) is input and the maximum switching frequency is recorded at which the output still resembles a square wave. This method gives a more realistic estimate of the frequency at which a digital circuit containing these transistors can operate. The two techniques of course operate in different regimes, since inverter switching is a large-signal effect, while transition frequency is a small-signal measurement. For this reason, the values of inverter switching frequency (blue diamonds) lag behind transition frequency (orange squares) as seen in Figure 12. Since transistor speed depends linearly on operating voltage, it is also instructive to normalize frequency by voltage (see Figure 12 (b)). The exponential trend of frequency improvement becomes more pronounced as it is otherwise partially masked by the recent trend towards lower operating voltage. One can note that the number of articles reporting high-frequency operation is smaller than the number of articles reporting scaled printing of OTFTs. This highlights the difficulty of achieving high-frequency operation, which requires dimensional scaling in terms of both channel length and electrode overlap as well as high material quality.

(a)



(b)

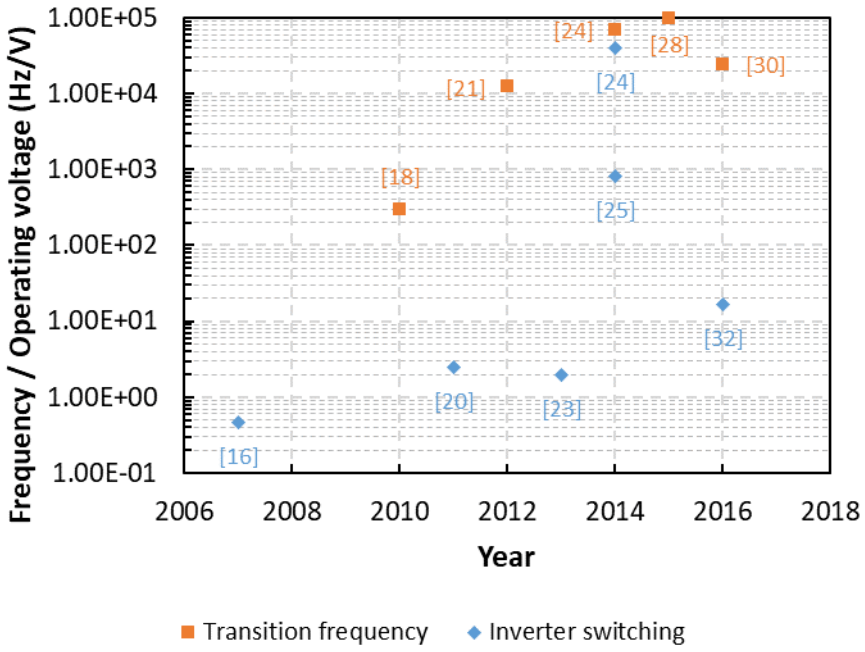


Figure 12. (a) Exponential improvement in transition frequency with a resistive load and inverter switching frequency with a load transistor. For articles that report ring oscillators, the switching frequency of a single inverter stage is plotted. (b) Switching frequency normalized by operating voltage shows a similar but more pronounced trend.

6. Conclusions

Printed organic thin-film transistors (OTFT) have experienced substantial dimensional scaling over the last decade. Lateral dimensions, channel length and overlap length, have been scaled successfully in a few different device architectures and using different combinations of printing methods. Operating voltage has been scaled less aggressively due to difficulties in achieving defect-free and thin gate dielectric films. Organic semiconductors have exhibited exponential improvement, mainly due to materials innovations, not dimensional scaling. However, the effect of electrode scaling on semiconductor performance needs to be considered to achieve the full potential of semiconductor materials. Combining these achievements has led to an exponential improvement in transistor switching frequency. To this point, there are several articles reporting high kHz to low MHz operation of high-speed printed OTFTs. These are important demonstrations, and are a promising first step towards integration into more complex circuits and realistic applications.

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